Model 875
Counter
Instruction Manual

This manual applies to instruments marked
"Rev 02" on rear panel

Rev Level 03
No Manual Change

WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Printed in U.S.A.

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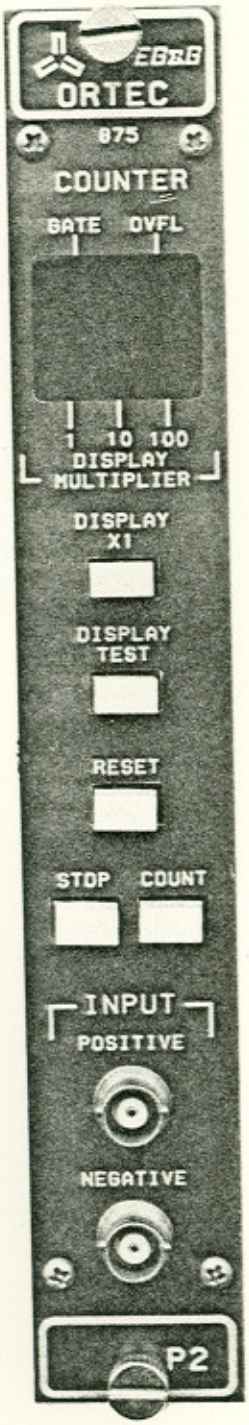
EG&G
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DISPLAY MULTIPLIER
DISPLAY X1
DISPLAY TEST
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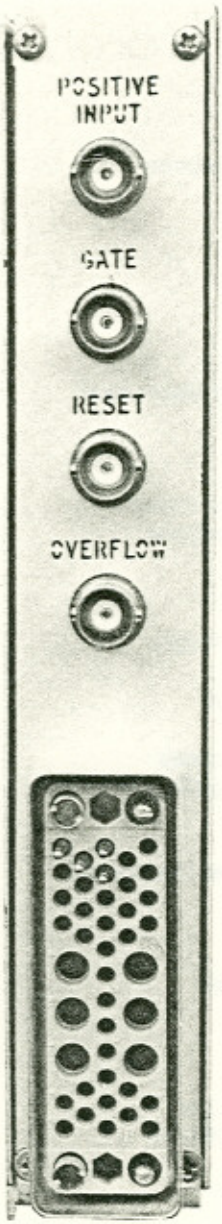
POSITIVE INPUT
GATE
RESET
OVERFLOW

1. DESCRIPTION

1.1. PURPOSE

The EG&G ORTEC 875 Counter is a modular, general-purpose counting instrument with a capacity of eight decades. Since only six decade digits are included in its display, the unit is auto-ranging and will display the six most significant digits of an accumulated count. A front panel switch permits the operator to shift the range and observe the six least significant digits at any time without interfering with the accumulation of additional counts.

The 875 counts both NIM-standard slow positive and fast negative input logic pulses. The input count rate is guaranteed to 25 MHz with a 40-ns pulse pair resolution. An overflow output pulse is provided for cascading counters when a capacity of more than eight decades is required.

1.2. GENERAL DESCRIPTION

The 875 is a NIM-standard single-width module that must be installed in a standard bin and power supply, such as the EG&G ORTEC 401/402 Series, for operation. Positive inputs can be furnished through either a front- or a rear-panel connector. Negative inputs are accommodated on the front panel only.

A Gate LED indicator in the digital display area of the front panel lights when the 875 is in a counting condition. The gate is controlled by Stop and Count pushbuttons on the front panel and by the rear panel Gate input circuit.

Reset is generated automatically when power is applied to the module from the bin and power supply. Reset can be provided manually by pressing the front panel Reset pushbutton at any time, whether the 875 is counting or not. Reset can also be provided at any time by a signal through the rear panel Reset connector.

The auto-ranging status is indicated by three LEDs that are included in the front panel display area. When the counter is reset, the LED for X1 is illuminated. As the count rate starts to accumulate, the X1 LED will remain illuminated until the number of counts exceeds 999 999. At a count level of 1 000 000, the LED for X10 illuminates to show that the display indicates the count level in decades 2 through 7. When the count level reaches 10 000 000, the display monitors decades 3 through 8 and the LED for X100 illuminates to show the status. At any time, the operator can press the Display X1 pushbutton and the display will monitor decades 1 through 6 without affecting the counting status of all eight decades. When the pushbutton is released, the 875 resumes its auto-ranging mode.

The six most significant digits are always displayed in the auto-ranging mode. By using the Display X1 pushbutton, all eight digits can be monitored regardless of the counting condition. Leading zero suppression is provided in the display until an overflow occurs. At each overflow, a positive logic pulse is furnished through the rear panel Overflow connector and can be used as the positive input to a second counting module. At the first overflow, the Overflow LED in the display area on the front panel illuminates and will remain on until the module is reset.

When the Display Test pushbutton is pressed, all seven segments in each digit in the display should light. The display reads 888 888 for this test regardless of the counting status or count level in the 875. It returns to the condition in which it monitors the count level when the switch is released.

2. SPECIFICATIONS

2.1. PERFORMANCE

COUNT CAPACITY 8 decades.

COUNTING RATE 25 MHz guaranteed.

PULSE PAIR RESOLUTION 40 ns minimum.

AUTOMATIC RESET Generated when power is applied.

2.2. INDICATORS

COUNTER DISPLAY Contains six characters, 7 LED segments per character.

X1 An LED illuminates when the unit displays decades 1 through 6 of the counter.

X10 An LED illuminates when the unit displays decades 2 through 7 of the counter.

X100 An LED illuminates when the unit displays decades 3 through 8 of the counter.

GATE An LED illuminates when the unit is in the counting condition.

OVFL An LED illuminates from the first overflow until reset.

2.3. CONTROLS

DISPLAY X1 Pushbutton switch that forces the unit to display decades 1 through 6 when depressed; unit returns to auto-ranging status when the switch is released.

DISPLAY TEST Pushbutton switch that illuminates all seven segments in each of the six characters in the display as a test function.

RESET Pushbutton switch that resets the counter to zero and turns off the OVFL LED (if illuminated).

STOP Pushbutton switch selects noncounting condition when depressed.

COUNT Pushbutton switch enables the counting condition when depressed; the counting condition can be inhibited by holding the Gate input below +1.5 V; Gate LED lights when counting condition is enabled.

2.4. INPUTS

POSITIVE Front and rear panel BNC connectors; either accepts positive unipolar or bipolar signals to ±10 V linear, 25 V max; threshold set at +1.5 V; minimum pulse width above threshold 20 ns. Z_{in} = 1K to ground, dc-coupled.

NEGATIVE Front panel BNC connector accepts fast negative logic pulses, 16 mA into 50Ω; threshold set at −250 mV; minimum pulse width over threshold 4 ns; input protected to ±25 V at 10% duty cycle.

GATE Rear panel BNC accepts standard slow positive logic or dc level to control counter input gate; >+3 V or open circuit allows counting; <+1.5 V inhibits counting; 25 V max; driving source must be capable of sinking 0.5 mA positive current during inhibit.

RESET Rear panel BNC accepts standard slow positive logic signal to cause counter reset to zero; >+3 V to reset; <+1.5 V or open circuit to not reset; 25 V max; pulse width >100 ns; Z_{in} = 2K to ground, dc-coupled.

2.5. OUTPUT

OVERFLOW Rear panel BNC provides a standard slow positive logic pulse at each overflow of the eight decade counter; Z_o <10Ω, dc-coupled and short-circuit protected.

2.6. ELECTRICAL AND MECHANICAL

POWER REQUIRED +24 V, 55 mA; −24 V, 0 mA; +12 V, 165 mA; −12 V, 60 mA.

DIMENSIONS NIM-standard single width module, 1.35 by 8.714 in. front panel, per TID-20893 (Rev).

3. INSTALLATION

3.1. GENERAL

The 875 Counter operates on input power that must be furnished from a NIM-standard Bin and Power Supply such as the EG&G ORTEC 401/402 Series. If any vacuum tube equipment is operated in the same rack with the 875, there must be sufficient cooling air circulating to prevent any localized heating of the integrated circuitry used throughout the 875. The temperature of equipment mounted in racks can easily exceed the maximum limit of 120°F (50°C) unless precautions are taken.

3.2. CONNECTION TO POWER

Turn off the Bin Power Supply when inserting or removing any modules. The EG&G ORTEC modules are designed so that it is not possible to overload the Power Supply with even a full complement of modules in the Bin. Since, however, this may not be true when the Bin contains modules other than those of EG&G ORTEC design, the Power Supply voltages should be checked after all modules have been inserted. The 401/402 has test points on the Power Supply control panel to permit monitoring the dc voltages easily.

When power is turned on for the Bin and Power Supply in which the 875 is installed for operation, the power is automatically turned on for the 875. When power is first applied, an automatic reset function in the 875 resets its counter to zero.

3.3. SIGNAL CONNECTIONS

COUNT INPUTS The 875 accepts and counts either fast negative logic pulses or slow positive logic pulses. Determine the type of input pulses that will be furnished and use the appropriate input connector.

Positive logic or analog signals can be connected to either the front or rear panel Positive input connector. These two connectors are **not isolated** from each other, so signals from two sources should not be connected simultaneously to the two Positive input connectors. The input circuit in the 875 is dc-coupled to eliminate baseline shifts associated with changing count rates. External capacitance coupling must be provided by the user for signals superimposed on a dc level greater than +1.5 V since the counter is designed to respond to signal transitions through the fixed threshold level of +1.5 V.

Negative logic signals must be furnished to the front panel Negative input connector. The input impedance in this circuit is 50Ω, dc-coupled. This is the standard impedance for which the fast negative logic pulse is defined.

There are two important points to remember when supplying signals to either input: (1) The signal should cross

the threshold level only one time. Signals with overshoot, ringing, etc., will be counted more than once if the discriminator level coincides with a level at which perturbations occur. (2) Signals with slow rise and fall times should be as clean (noise free) as possible because of the high gain and bandwidth of the 875 discriminator. As a slow signal approaches the threshold, a small spurious noise pulse can traverse the threshold and return, causing an extra count to be added to the contents of the counter.

GATE INPUT A gate input signal or dc level can be connected to the 875 through the rear panel connector. With no connections made to this BNC, the input voltage level is about +3 V and the counter gate will permit the unit to operate. To cut off the gate, the signal input must be pulled down to below +1.5 V. To do this, the driving circuit must be capable of absorbing 0.5 mA from the gate input circuit. The gate circuit will permit counting when the signal level is +3 V or greater.

RESET INPUT A reset input signal can be connected to the 875 through the rear panel BNC Reset connector. To reset the counter to zero, a positive signal of 3 V or greater, with a minimum width of 100 ns, must be used. The input impedance is approximately 2K to ground. Negative signals will not perform any useful function at the Reset input.

OVERFLOW OUTPUT The Overflow signal is available through the Overflow BNC on the rear panel. A slow positive logic signal appears at this connector each time the contents of the counter change from 99 999 999 to 0. The output signal is 500 ns wide. Z_o is less than 10Ω, dc-coupled. To increase the counting capacity beyond the eight decades that are included in the 875, furnish this output signal as the positive input into another counting module.

4. OPERATION

After the 875 has been installed according to the information in Section 3, no further operating adjustments are required. Each input pulse within specifications that is furnished while the 875 is in a counting condition will be counted and displayed.

If there is a power interruption, the 875 will be automatically reset when the power is restored. The counter can be reset to zero by using the front panel pushbutton switch or by furnishing an input pulse through the rear panel Reset connector.

Each accepted input pulse will add one count to the previous count level that is in the counter, regardless of whether the counting period has been interrupted, gated, or otherwise caused to be discontinuous. The contents of the counter are not affected by use of the Display Test switch or the Display X1 switch, although each of these switches does affect the actual characters shown in the display.

5. CIRCUIT DESCRIPTION

5.1. GENERAL

The schematic for the EG&G ORTEC 875 Counter is 875-0201-S1, included at the back of this manual. The circuits are included on the main printed circuit board and on a printed circuit board that is installed on the front panel. The 875 is designed to accommodate computer-aided testing, using the test points that are identified in the schematic.

5.2. COUNTER INPUT

Integrated circuit IC13 is a dual discriminator. One section is used for positive inputs and the other for negative inputs. The positive input threshold is set by R50 and R53, while the negative input threshold is set by R48 and R52. The positive input impedance is set by R49 and R51 at 1K, and these resistors also divide the input signal by two and protect the comparator to ±25 V. Negative input protection is provided by R9, R46, R59, D1, D3, and C23. Transistors Q1 and Q2 stretch the negative input signal on C20 for a sufficient time to permit IC13 to change states. The time constant is set by R45 and C20 such that a pulse pair resolution of less than 40 ns can be achieved while allowing a 4 ns wide fast NIM signal to be counted.

5.3. PULSE SHAPER

Integrated circuit IC3 is connected as a positive edge triggered monostable. Any input signal through IC13, from either the positive or the negative input circuit, will be furnished to pin 3 of IC3 to trigger the monostable. The pulse width is set at about 20 ns by R42 and C17. As long